IEEE VLSI Based projects based on verilog and Xilinx.

Communication

1. Block Inter-leaver Design for High Data Rate Wireless Networks

With increasing data rates in wireless communication, quality of service (QoS) has become a major issue. This is more with fading channels transmitting huge volumes of data. QoS is degraded by intersymbol interference (ISI) and related errors. One of the simplest and convenient techniques to overcome such errors is interleaving, which is used efficiently in wireless applications. It has found applications for combating burst errors that creeps up in the channel during transmission. In this paper, an efficient model of a block interleaver using a hardware description language (Verilog) is proposed. The proposed technique reduces consumption of FPGA resources to a large extent, which implies low power consumption.

2. A Novel Reconfigurable Architecture For Generic OFDM Modulator Based On FPGA

OFDM is a special case of multi-carrier modulations, which is of great use in various wireless communications, such as DAB, DVB, HDTV, CMMB, TMMB, 802.11a. The OFDM frame structure is similar to each other. It consists of a number of OFDM symbols following the synchronizing signal with different cyclic prefix and guard interval. In this case, it is significant for researchers to implement OFDM modulator through a novel reconfigurable architecture to meet different communication standards. This paper shows how the architecture is realized on FPGA.

3. Implementation and Evaluation of a High-Performance MIMO Detector for Wireless LAN Systems

This paper presents the implementation and experimental evaluation of an advanced MIMO detector for wireless LAN systems. The proposed detector architecture is based on the well-known lattice-reduction aided MMSE method. Several optimizations at both algorithmic and architectural level are presented which result in an efficient VLSI design able to meet the timing requirements of a practical OFDM-based wireless LAN receiver while keeping complexity at moderate levels. Moreover, the detector offers built-in compensation for transmitter impairments such as nonlinear power amplifier characteristics, hence providing a full and cost-effective solution for practical systems. The described solution is implemented on an FPGA-based IEEE802.11n prototype and evaluation results comparing performance of both conventional MMSE and reduced-lattice detection under several propagation scenarios are presented. Experimental results show significantly lower error rates at the receiver for the advanced detector, or equivalently a lower number of required receiver antenna elements for a given performance target, hence resulting in lower cost, physical size and energy consumption1

4. Comparative analysis of different hardware decoder architectures for IEEE 802.11ad LDPC code

This paper considers the LDPC code designed for the IEEE 802.11ad WLAN standard and analyzes different architectural options for the hardware decoder. Three decoder architectures are studied that provide different tradeoffs between the throughput and the required amount of the resources for the

FPGA implementation. The standard fully parallel decoder is demonstrated to have the maximum throughput of above 6.5 Gbit/s and also the maximum hardware efficiency (a ratio of the decoder throughput to the amount of the consumed hardware logic). The layered decoder architecture allows reusing the hardware check nodes blocks between the sub-iterations to achieve 46% lower hardware resources utilization relative to the fully parallel decoder though at the expense of the 42% lower hardware efficiency and providing the throughput of 2.1 Gbit/s. The serial-parallel decoder architecture exploits the layered and quasi-cyclic properties of the code matrix and occupies only 11% of the hardware resources needed by the fully parallel decoder but with the throughput of only 159 Mbit/s.

5. Reconfigurable FFT using CORDIC based architecture for MIMO-OFDM receivers

Fast Fourier Transform (FFT) is one of the most important algorithm in signal processing and communications and is used in orthogonal frequency division multiplexing (OFDM) systems. FFT are the crucial computational blocks to perform the baseband multicarrier demodulation in a MIMO OFDM system and the hardware complexity will be very high. This paper proposes a CORDIC based reconfigurable 64 point Fast Fourier Transform which is used for various IEEE standard based WLAN receivers. The CORDIC based FFT block minimizes the hardware complexity because of the elimination of multiplier units and twiddle factors. This design has the minimal hardware and computational complexity to meet the IEEE standard. In this paper, a reconfigurable FFT has been realized based on CORDIC architecture. The coding for reconfigurable 64 point FFT has been done using VHDL under Xilinx platform. The results are verified and are found to be compatible with Virtex xc6vcx240t-2ff704.