

VLSI PROJECT ABSTRACTS

Network Security & Cryptographic Sciences, Digital Signal Processing, Arithmetic Core and Digital Electronics, Digital Communications and Information theory, Digital Image Processing, Bus Protocols and System on Chip

IEEE VLSI Based projects based on verilog and Xilinx.

Signal Processing

1. Investigation in FIR Filter to Improve Power Efficiency and Delay Reduction.

In design of Finite Impulse Response (FIR) filter using adder, coefficients and multiplication are used. Multiple Constant Multiplication (MCM) is the algorithm which is used in FIR designing to minimize complexity of the circuit, increased delay and multiplication using large area. These problems can be optimized by using new technique known as digit-serial multiple constant multiplications. It reduces the complexity, delay and area utilization. Along with this already existed method, the modified carry select adder implemented in the current paper. It shows that there should be 10-20% increment in power efficiency and 50% reduction in delay compared to already exist techniques.

Index Terms— CSA; Delay; FIR filter; GB; MCM; VLSI.

2. A Reconfigurable Overlapping FFT/IFFT Filter for ECG Signal De-noising

Dynamic Electrocardiograph (ECG) monitoring (known as Holter) plays an important role in the earlier detection and diagnosis of various cardiovascular diseases. ECG signals obtained from Holter systems normally contain a lot of noises and artifacts. These noises degrade signal quality, which may be critical for routine monitoring and diagnosis. To solve the problem, a reconfigurable overlapping fast Fourier transform/ inverse fast Fourier transform (FFT/IFFT) filter for suppressing the power-line interference and the high-frequency noise is presented in this paper. The filter is based on a 12-lead Holter system with a high-performance analogue front-end and a field-programmable gate array (FPGA) for enhanced digital processing. This paper analyzes the performance of the reconfigurable overlapping FFT/IFFT filter in ECG de-noising applications and validate it by real-world emulations. Furthermore, the de-noising performance of the reconfigurable overlapping FFT filter was evaluated.

3. High-Throughput Programmable Systolic Array FFT Architecture and FPGA Implementations

A small, fine-grained systolic FFT architecture is described that is fast, programmable, can do non-power-of-two DFTs, and provides a higher signal-to-noise ratio for a given fixed-point word length than traditional block floating point approaches. To demonstrate the basic architecture, several designs were implemented using 65nm FPGA technology: (1) fixed-size 256-point and 1024-point circuits; (2) a power-of-two variable FFT circuit for LTE OFDM; and (3) a non-power-of-two circuit for LTE SC-FDMA DFT computations, that is programmed by entering parameter values into a single ROM memory. These three circuits demonstrate >37%, 62% and >100% higher throughputs than the other pipelined and memory-based FFTs to which they are compared. These circuits run at clocks speeds as high as 566 MHz, 46% higher than any other circuit in the comparisons. Finally, the architecture provides scalable throughput by increasing the array size.

4. FPGA based partial reconfigurable fir filter design

This paper proposes partial reconfigurable FIR filter design using systolic Distributed Arithmetic (DA) architecture optimized for FPGAs. To implement computationally efficient, low power, high speed Finite Impulse Response (FIR) filter a two dimensional fully pipelined structure is used. To reduce the partial reconfiguration time a new architecture for the Look-Up Table (LUT) in distributed arithmetic is proposed. The FIR filter is dynamically reconfigured to realize low pass and high pass filter characteristics by changing the filter coefficients in the partial reconfiguration module. The design is

#56, II Floor, Pushpagiri Complex, 17th Cross 8th Main, Opp Water Tank, Vijaynagar, Bangalore-560040.

Website: www.citlprojects.com, Email ID: citlprojectsieee@gmail.com, projects@citlindia.com

MOB: 9886173099, Whatsapp: 9986709224, PH : 080 -23208045 / 23207367.

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5. On the 2×2 DFT-spread Space-Time Block Code COOFDM for PDM optical communications

This work presents the combining of two methods, which are discrete Fourier transform spread (DFT-spread) and 2×2 space time block codes (STBC), to improve the system performance for polarization division multiplexing (PDM) coherent optical orthogonal frequency division multiplexing (CO-OFDM) communication systems. The system performances are generally measured by the unit of bit error rate (BER). For 64-QAM, the communication length of 850 km can be achieved at the forward error control (FEC) limit.

6. Design and Implementation of FPGA - Digital Based PID Controller

The main aim of this paper is to design an effective realization of digital PID control algorithms using fieldprogrammable gate array (FPGA) technology. The proportional \square integral \square derivative (PID) control methods and algorithms are one of the most common types of effective feedback controllers that are used in automatic control in many industrial processes. PID controller has been widely used in many different areas, such as power systems, drives control, automotive mechatronics, aerospace, process control, and robotics. Implementation of PID control algorithms has gone through several stages of realization, from early mechanical, electrical and pneumatic designs to microprocessor-based systems. Recently, field-programmable gate arrays (FPGAs) have become an alternative solution for the realization of digital control algorithm systems, which were previously dominated by general-purpose microprocessor systems. In comparison with convention PID realization, FPGA- complex functionality, and low power consumption. Another advantage of FPGA-based platforms is their capability to execute concurrent operations, allowing parallel architectural design of different digital controllers system. In the propose paper we demonstrate of the one application of hardware and software module development for the application and realization of digital PID control algorithm for dynamical systems with fast dynamics. We successfully implemented verified and analyze the FPGA PID control algorithm realization for high speed DC motors using FPGA technology (Spartan - 6 FPGA Family of company Xilinx) which delivers an optimal balance of low risk, low cost, and low power for this applications.

7. Fault Tolerant Parallel Filters Based on Error Correction Codes

Digital filters are widely used in signal processing and communication systems. In some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. Over the years, many techniques that exploit the filters' structure and properties to achieve fault tolerance have been proposed. As technology scales, it enables more complex systems that incorporate many filters. In those complex systems, it is common that some of the filters operate in parallel, for example, by applying the same filter to different input signals. Recently, a simple technique that exploits the presence of parallel filters to achieve fault tolerance has been presented. In this brief, that idea is generalized to show that parallel filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC. This new scheme allows more efficient protection when the number of parallel filters is large. The technique is evaluated using a case study of parallel finite impulse response filters showing the effectiveness in terms of protection and implementation cost.

8. Analysis and Implementation of Low-cost FPGA Based Digital Pulse-width Modulators

This paper describes the architecture and operating principles of two digital pulse-width modulator (DPWM) implementations for low-cost field-programmable gate arrays (FPGAs). Both architectures are based on a countercomparator block to process the most significant bits (MSB) portion of the reference input, enriched with additional elements to enhance duty-cycle resolution according to the

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less significant bits (LSB). The first architecture described has already been reported in the literature, it uses the on-chip PLL blocks to generate fixed delays and a selector to choose the one corresponding with the desired duty-cycle. Post-fitting adjustments of PLL delays are required to compensate delay differences between the diverse signal paths across the selector. In the second architecture described, a serializer-deserializer (SERDES) module is used to serialize a thermometer-coded representation of the LSB portion of the input. This serialization technique is commonly used for data transmission on high-speed serial I/O data transmission standards like LVDS and is extensively supported by FPGA providers. Experimental results are presented for both architectures synthesized on standard low-cost FPGA chips, showing very good linearity and resolutions up to 1ns. The first architecture provides a moderately better resolution. The second architecture, on the other hand, is a much more robust solution as it requires no post fitting delay adjustments.

9. A Review on FPGA Based Pulse Processing System

In process to create a more suitable and accurate pulse processing system FPGA system is developed. Analog system takes wide space for pulse processing. FPGA technology has replaced this disadvantage. It has become an extremely cost-effective means of off-loading computationally intensive digital signal processing algorithms to improve overall system performance. The digital filter implementation in FPGA, utilizing the dedicated hardware resources can effectively achieve application-specific integrated circuit (ASIC)-like performance while reducing development time cost and risks. A low-pass filter can be implementing on FPGA. MATLAB tool with FPGA system is best way to design digital system.

10. An FPGA Implementation of Frequency Output

Digital frequency input and output (typically in the range 1 Hz to 100 kHz) for data transmission are employed in many industrial applications. This paper provides the following elaborations of the ISIE'07 conference paper. A thorough literature review suggests that previous techniques can be classified into three basic approaches. Theoretical expressions for the errors of each are derived and compared with the new approach developed by the authors. Each method has been implemented in a more recent field programmable gate array architecture (Spartan 3), and the results are consistent with the theoretical values. The new method provides a precision of $6 \times 10^{-6}\%$ or better for all frequencies, based on a 40-MHz clock.

11. Low Latency Systolic Montgomery Multiplier for Finite Field Based on Pentanomials

In this paper, we present a low latency systolic Montgomery multiplier over based on irreducible pentanomials. An efficient algorithm is presented to decompose the multiplication into a number of independent units to facilitate parallel processing. Besides, a novel so-called "pre-computed addition" technique is introduced to further reduce the latency. The proposed design involves significantly less area-delay and power-delay complexities compared with the best of the existing designs. It has the same or shorter critical-path and involves nearly one-fourth of the latency of the other in case of the National Institute of Standards and Technology recommended irreducible pentanomials.

12. Design and FPGA Implementation of Linear FIR Low-pass Filter Based on Kaiser Window Function.

Aiming at the requirements of real time signal processing, a cut-off frequency of 100 KHz, 16-tap direct form FIR linear-phase low-pass filter using Kaiser Window function was designed out based on DSP Builder system modeling approach. The signal waveforms in time domain and frequency domain before and after filtering were analyzed. Ultimately, a highest response frequency of 61.71MHz high-speed

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FIR low-pass filter was implemented on EP2C35F672C8 FPGA. Design efficiency and filter performance has been greatly improved.

13. FPGA Implementation of Adaptive LMS Filter

The adaptive filter constitutes an important part of the statistical signal processing. Whenever there is a requirement to process signals that result from operation in an environment of unknown statistics, the use of an adaptive filter offers an attractive solution to the problem as it usually provides a significant improvement in performance over the use of a fixed filter designed by conventional methods. Furthermore, the use of adaptive filters provides new signal-processing capabilities that would not be possible otherwise. We thus find that adaptive filters are successfully applied in such diverse fields as